REMARKS

Claims 1-20 are pending. Claims 9-12, 17-18 and 20 have been amended. In view of the following, all pending claims are in condition for allowance. If, after considering this response, the Examiner does not agree that all of the claims are allowable, he is requested to schedule a teleconference with the Applicants' attorney to further the prosecution of the application.

Rejection of claims 1-8 under 35 U.S.C. §112, second paragraph

Claim 1

Claim 1 recites a first means for turning off the switch with a turn-off delay, and a second means for turning on the switch with a turn-on delay shorter than the turn-off delay.

For example, referring, *e.g.*, to FIG. 4 and paragraphs [53]-[61] of the present application, a first means 88 turns off the switch 81 with a turn-off delay, and a second means 86 turns on the switch 81 with a turn-on delay shorter than the turn-off delay.

On pages 2-4 of the office action, the Examiner states that the cited language is absent from the disclosure. However, it is clear from the disclosure that the "first means" is resistor 88, the "second means" is resistor 86, and the "switch" is transistor 81. Paragraph [56] clearly states that "transistor 81 remains on for as long as resistor 88 has not discharged its gate capacitance." Paragraph [56] also clearly states that "the turning-on of transistor 81 is conditioned by the charge of its gate capacitance through resistor 86." Finally, paragraph [61] clearly supports the cited language of claim 1 by stating that "since resistor 86 has a value smaller than that of resistor 88, the turning-on is faster than the turning-off." Therefore, there is adequate disclosure showing what is meant by "second means" in claim 1.

Claims 2-8

Claims 2-8 are patentable by virtue of their dependencies from claim 1.

Rejection of claims 1 and 3-5 under 35 U.S.C. §102(b) as being anticipated by Pechlaner et al. (DE 199 28 760)

Claim 1

Claim 1 recites a device for protecting a circuit against a polarity reversal, the device comprising a first means for turning off a switch with a turn-off delay, and a second means for turning on the switch with a turn-on delay shorter than the turn-off delay.

For example, referring, *e.g.*, to FIG. 4 and paragraphs 53-61 of the present application, a device 8 protects a circuit 1 against a polarity reversal. The device 8 comprises a first means 88 for turning off a switch 81 with a turn-off delay, and a second means 86 for turning on the switch 81 with a turn-on delay shorter than the turn-off delay.

Pechlaner, on the other hand, does not disclose a device for protecting a circuit against a polarity reversal, the device comprising a first means for turning off a switch with a turn-off delay, and a second means for turning on the switch with a turn-on delay shorter than the turn-off delay. On page 7 of the office action, the Examiner mistakenly interprets the smart power switch 5 of Pechlaner as the "controllable switch" within the polarity protection device. However, Pechlaner clearly states in the third and fourth paragraphs on page 8 of the English translation that the smart power switch 5 is the circuit being protected ("to protect all smart power switches in the event of the wrong polarity"), and that the polarity protection device consists of "the MOSFET 6, the resistor 7, the capacitor 9, and the Zener diode 10." As a result, the smart power switch 5 is not the polarity protection device, but instead the circuit to be protected. Furthermore, the smart power switch 5 is simply interposed between the first power supply terminal 1 and the ground terminal GND. Or in the alternative, the smart power switch 5 is simply interposed between the first power supply terminal 1 and the load 11, which is connected to the second power supply terminal 2 (page 8 of Pechlaner clearly lists terminals 1 and 2 as first and second power supply terminals for Vbb). Either way, the smart power switch 5 is not interposed between a first terminal of the DC power supply and a first terminal of the circuit that it is protecting. The smart power switch 5 does not

in any way protect the ground GND, the load 11, or the power supply Vbb against a polarity reversal.

Because Pechlaner clearly establishes the smart power switch 5 as the circuit to be protected (and not the polarity protection device), we now look at the MOSFET 6, the resistor 7, the capacitor 9, and the Zener diode 10 (which Pechlaner clearly establishes as the polarity protection device). However, the polarity protection device of Pechlaner does not comprise the turning-off and turning-on means as recited in claim 1. Only the switch 6 can be interpreted as the "controllable switch", but even if the capacitor 9 introduces a delay for turning off the switch 6 in the presence of a reverse polarity, the switch 6 is not turned on with a delay as recited in claim 1. In fact, contrary to what the Examiner states on page 7 of the office action, there is no control signal coming from a controller to the switch 6. Instead of a controller, the gate of the switch 6 is directly connected to the power supply Vbb through the resistor 7.

Therefore, Pechlaner does not satisfy all of the limitations of claim 1.

Claims 3-5

Claims 3-5 are patentable by virtue of their dependencies from claim 1.

Rejection of claims 2 and 6-8 under 35 U.S.C. §103(a) as being unpatentable over Pechlaner

Claims 2 and 6-8 are patentable by virtue of their dependencies from claim 1.

Rejection of claims 9-20 under 35 U.S.C. §103(a) as being unpatentable over Pechlaner in view of Yamada et al. (US 5,726,505)

Claim 9

Claim 9, as amended, recites a switch operable to conduct a current to a first node of a power supply when the first node has a predetermined polarity relative to a second node of the power supply, and a first delay element coupled to the switch and operable to disable the switch from conducting current at a predetermined time after the polarity reverses.

For example, referring, *e.g.*, to FIGS. 2 and 4 of the present application, a switch 81 is operable to conduct a current to a first node 32 of a power supply Vbat when the first node 32 has a predetermined polarity relative to a second node 31 of the power supply Vbat. A first delay element (82, 88) is coupled to the switch 81 and is operable to disable the switch 81 from conducting current at a predetermined time after the polarity reverses. It should be noted that the first delay element (82, 88), as defined throughout the present application, is an actual circuit element with its own circuit symbol in a circuit diagram. A "circuit element" as known in the art is not a direct wire connection. A "circuit element" as known in the art must constitute an element (such as a resistor, capacitor, inductor, etc.) in addition to the direct wire connection.

Pechlaner, on the other hand, does not teach a first delay element coupled to the switch and operable to disable the switch from conducting current at a predetermined time after the polarity reverses. The Examiner interprets the semiconductor switch 3 of Pechlaner as the "switch" on pages 9-10 of the office action. However, there is no circuit element coupled between the control device 4 and the switch 3. There is only a direct wire connection between the control device 4 and the switch 3. The "first delay element" recited in claim 9 of the present application is actually a circuit element as known in the art. Furthermore, the Examiner concedes on page 6 of the Office Action that Pechlaner fails to describe any of the circuitry within the control device 4. As a result, not only does Pechlaner fail to teach any circuitry within the control device 4 to disable the switch 3 after a polarity reversal, but Pechlaner fails to teach any circuitry within the control device 4 to disable the switch 3 at a predetermined time after a polarity reversal.

Similarly, Yamada (not Yoshida) does not teach any of the shortcomings of Pechlaner. Instead, Yamada teaches a current detector 6 that detects a current flowing from a solar power supply 1 to a battery power supply 2 (FIGS. 1-2). If this current flowing from the solar power supply 1 to the battery power supply 2 falls below a certain level, the current detector 6 opens MOSFET 5 to prevent current from ever flowing from the battery power supply 2 to the solar power supply 1 (col. 5, lines 19-56). However, this all has nothing to do with the polarity reversal of a single power supply. Neither the solar power supply 1 nor the battery power supply 2 ever reverses polarity. Both the

solar power supply 1 and the battery power supply 2 always maintain their polarity, only the amount of current that flows from the solar power supply 1 to the battery power supply 2 changes (the direction of this current does not change because of MOSFET 5). As a result, not only does Yamada fail to teach any circuitry to disable a switch at a predetermined time after a polarity reversal, but Yamada fails to teach any kind of power supply polarity reversal whatsoever.

Therefore, not only is there no motivation to combine the teachings of Pechlaner and Yamada, but the combination of Pechlaner and Yamada does not even satisfy all of the limitations of claim 9.

Claims 13, 17-18 and 20

Claims 13, 17-18 and 20, as amended, are patentable for reasons similar to those recited above in support of the patentability of claim 9.

Claims 10-12, 14-16 and 19

Claims 10-12, 14-16 and 19 are patentable by virtue of their respective dependencies from claims 9, 13 and 18.

CONCLUSION

In light of the foregoing, claims 1-20 are in condition for allowance, which is respectfully requested.

If, after considering this response, the Examiner does not agree that all of the claims are allowable, then it is respectfully requested that the Examiner schedule a phone interview with the Applicants' attorney at (425) 455-5575.

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Respectfully submitted,

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